IN THE SPECIFICATION

Please amend the specification as follows:

[0022] Figure 4 shows a ~~plane~~ plan view of an array capacitor according to one embodiment. Specifically, Figure 4 shows a section surface on which a second conductive layer 202 is disposed. The first conductive vias 331, 333, 335 pass through the second conductive layer 202, which form gaps 401, 403, 405 around the part where the first conductive vias 331, 333, 335 pass through. In an embodiment, the first conductive vias 331, 333, 335 are insulated from the second conductive layer 202. The second conductive layer 202 is connected to other second conductive layers by the second conductive vias 334, 336.

[0024] Figure 5 shows a process of incorporating an array capacitor into an integrated circuit package according to one embodiment. In block 510, an array capacitor with voids is provided. This may be done by fabricating a complete array capacitor and then forming voids or holes in the array capacitor ~~subsequent to~~during the fabrication of the array capacitor. The voids or holes formed in the array capacitor are arranged to coincide with the pins extending from the IC package. Then in block 520, an integrated circuit housed by an IC package is provided. The array capacitor is positioned with respect to the IC package by passing the IC package pins through the openings formed in the array capacitor such that the array capacitor is located directly underneath the integrated circuit mounted on the IC package (block 530). Then, the array capacitor is electrically connected to the IC package by using the conductive terminals provided on the array capacitor to couple with the ground plane and power plane provided in the IC package (block 540). Then in block 550, the IC package and the array capacitor is connected to a socket on a printed circuit board.

CONCLUSION

The specification has been amended to correct minor informalities and no new matter has been added. If there are any fees due in connection with the filing of this response, please charge those fees to our Deposit Account No. 02-2666.

Respectfully submitted,

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Dated: 6/23/04

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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Marilyn Bass — 06.23.04 — Date